**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| In re Patent Application of | ) | |
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| Shinichi Takagi et al. | ) | Group Art Unit: 2823 |
| | ) | |
| Application No.: 09/987,153 | ) | Examiner: SHEILA V CLARK |
| | ) | |
| Filed: November 13, 2001 | ) | Appeal No.: _____ |
| | ) | |
| For: SEMICONDUCTOR ELEMENT MODULE AND SEMICONDUCTOR DEVICE WHICH PREVENTS SHORT CIRCUITING | ) | |

## APPEAL BRIEF

**Mail Stop APPEAL BRIEF - PATENTS**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This appeal is from the decision of the Primary Examiner dated April 7, 2008 finally rejecting claims 11-47, 51-54 and 56-62, which are reproduced in the Claims Appendix of this brief.

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The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.17 and 41.20 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 024800.

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## I. Real Party in Interest

The present application is assigned to Mitsubishi Denki Kabushiki Kaisha, who is the real party in interest.

## II. Related Appeals and Interferences

No other appeal, interference or judicial proceeding is known which will affect or be directly affected by, or have bearing on, the Board's decision in this appeal.

## III. Status of Claims

The reissue application involved in this appeal contains claims 1-62. Claims 1-10 are the claims that issued in the original patent, and are presumed to be allowed since there is no rejection of these claims in the final Office Action dated April 7, 2008.[1]

Claims 11-62 were presented with the reissue application. Of these, claims 48-50 and 55 have been canceled. Claims 11-47, 51-54 and 56-62 are pending, and stand finally rejected. All of these finally rejected claims are being appealed.

## IV. Status of Amendments

An Amendment was filed on September 8, 2008, amending the claims to adopt the Examiner's suggestion set forth in the final Office Action. In the Advisory Action dated October 9, 2008, entry of the Amendment was refused.

Appellants hereby withdraw the Amendment filed September 8, 2008.

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[1] The first Office Action dated August 29, 2003 contained a rejection of claims 1-10 under 35 USC 251 on the basis of a defective reissue declaration. Appellants' response to that Office Action provided a Supplemental Declaration to remove the basis for the rejection. Since that time, original claims 1-10 have not been addressed in the Office Actions, but the rejection based upon the allegedly defective declaration has not been repeated, and there have been no other rejections of claims 1-10.

V. Summary of Claimed Subject Matter

Independent claim 11 recites a semiconductor element module **(shown in each of Figures 1A-6B; column 3, lines 19-45)**, comprising

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)**;

a semiconductor element within said package ***(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)***;

a plurality of leads **(Figs. 3A and 3B, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Fig. 3B, vertical portion of the leads 6)** and another open end portion bent in an outward direction relative to the side surface of said package **(Fig. 3B, horizontal portion of the leads 6)**, said open end portion being downwardly protruded from a plane including a bottom surface of said package **(Fig. 3B, the horizontal portion is lower than the bottom surface of the package 4)**; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 3A and 3B, element 12; column 4, lines 37-40)**.

Independent claim 16 recites a semiconductor device comprising a substrate **(Figs. 3A and 3B, element 8; column 1, lines 33-35; column 4, line 35)** and a semiconductor element module mounted on said substrate, said semiconductor element module including:

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)**;

a semiconductor element within said package ***(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)***;

a plurality of leads **(Figs. 3A and 3B, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Fig. 3B, vertical portion of the leads 6)** and another open end portion bent in an outward direction relative to the side surface of said package **(Fig. 3B, horizontal portion of the leads 6)**, said open end portion being downwardly

protruded from a plane including a bottom surface of said package **(Fig. 3B, the horizontal portion is lower than the bottom surface of the package 4)**; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 3A and 3B, element 12; column 4, lines 37-40)**.

Independent claim 21 recites a semiconductor element module, comprising:

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)** having an opening for allowing an optical signal to pass therethrough **(Fig. 1, opening in package 4 through which optical fiber 2 passes)**;

an optical element located in said package for outputting or inputting the optical signal **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 3A and 3B, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Fig. 3B, vertical portion of the leads 6)** and another open end portion bent in an outward direction relative to the side surface of said package **(Fig. 3B, horizontal portion of the leads 6)**, said open end portion being downwardly protruded from a plane including a bottom surface of said package **(Fig. 3B, the horizontal portion is lower than the bottom surface of the package 4)**; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 3A and 3B, element 12; column 4, lines 37-40)**,

each of said leads having an uppermost end which is lower than an uppermost end of said opening **(Figs. 3A and 3B, Figs. 6A and 6B; top end of leads 6 is lower than top of hole in package 4)**.

Independent claim 22 recites a semiconductor element module, comprising;

a package having an inner bottom surface **(Figure 1A *et seq.*, element 4; column 4, line 13)** and an opening for allowing an optical signal to pass

therethrough **(Fig. 1, opening in package 4 through which optical fiber 2 passes)**;

an optical element located in said package for outputting or inputting the optical signal **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 3A and 3B, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Fig. 3B, vertical portion of the leads 6)** and another open end portion bent in an outward direction relative to the side surface of said package **(Fig. 3B, horizontal portion of the leads 6)**, said open end portion being downwardly protruded from a plane including a bottom surface of said package **(Fig. 3B, the horizontal portion is lower than the bottom surface of the package 4)**; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 3A and 3B, element 12; column 4, lines 37-40)**,

each of said leads having an uppermost end which is lower than an uppermost end of said opening **(Figs. 3A and 3B, Figs. 6A and 6B; top end of leads 6 is lower than top of hole in package 4)**, said level difference having a surface which intersects the side surface of said package, and the surface of said level difference being higher than the inner bottom surface of said package **(Fig. 1C, upper surface of level difference 12 is higher than inner bottom surface of package 4)**.

Independent claim 24 recites a semiconductor device comprising a substrate **(Figs. 3A and 3B, element 8; column 1, lines 33-35; column 4, line 35)** and a semiconductor element module mounted on said substrate,

said semiconductor element module including;

a package having an inner bottom surface **(Figure 1A *et seq.*, element 4; column 4, line 13)** and an opening for allowing an optical signal to pass therethrough **(Fig. 1, opening in package 4 through which optical fiber 2 passes)**;

an optical element located in said package for outputting or inputting the optical signal **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 3A and 3B, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Fig. 3B, vertical portion of the leads 6)** and another open end portion bent in an outward direction relative to the side surface of said package **(Fig. 3B, horizontal portion of the leads 6)**, said open end portion being downwardly protruded from a plane including a bottom surface of said package **(Fig. 3B, the horizontal portion is lower than the bottom surface of the package 4)**; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 3A and 3B, element 12; column 4, lines 37-40)**,

each of said leads having an uppermost end which is lower than an uppermost end of said opening **(Figs. 3A and 3B, Figs. 6A and 6B; top end of leads 6 is lower than top of hole in package 4)**, said level difference having a surface which intersects the side surface of said package, and the surface of said level difference being higher than the inner bottom surface of said package **(Fig. 1C, upper surface of level difference 12 is higher than inner bottom surface of package 4)**.

Independent claim 25 recites a semiconductor element module, comprising;

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)** having an opening for allowing an optical signal to pass therethrough **(Fig. 1, opening in package 4 through which optical fiber 2 passes)**;

an optical element located in said package for outputting or inputting the optical signal **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a mount having said optical element placed thereon for fixing said optical element to said package **(Fig. 1B, element 3; column 1, lines 20-21; column 4, lines 1-3)**;

a plurality of leads **(Figs. 3A and 3B, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Fig. 3B, vertical portion of the leads 6)** and another open end portion bent in an outward direction relative to the side surface of said package **(Fig. 3B, horizontal portion of the leads 6)**, said open end portion being downwardly protruded from a plane including a bottom surface of said package **(Fig. 3B, the horizontal portion is lower than the bottom surface of the package 4)**; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 3A and 3B, element 12; column 4, lines 37-40)**,

each of said leads having an uppermost end which is lower than an uppermost end of said opening **(Figs. 3A and 3B, Figs. 6A and 6B; top end of leads 6 is lower than top of hole in package 4)**, said level difference having a surface which intersects the side surface of said package, and the surface of said level difference being higher than a bottom surface of said mount **(Fig. 1C, upper surface of level difference 12 is higher than bottom of mount 3)**.

Independent claim 27 recites a semiconductor device comprising a substrate **(Figs. 3A and 3B, element 8; column 1, lines 33-35; column 4, line 35)** and a semiconductor element module mounted on said substrate,

said semiconductor element module including;

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)** having an opening for allowing an optical signal to pass therethrough **(Fig. 1, opening in package 4 through which optical fiber 2 passes)**;

an optical element located in said package for outputting or inputting the optical signal **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a mount having said optical element placed thereon for fixing said optical element to said package **(Fig. 1B, element 3; column 1, lines 20-21; column 4, lines 1-3)**;

a plurality of leads **(Figs. 3A and 3B, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Fig. 3B, vertical portion of the leads 6)** and another open end portion bent in an outward direction relative to the side surface of said package **(Fig. 3B, horizontal portion of the leads 6)**, said open end portion being downwardly protruded from a plane including a bottom surface of said package **(Fig. 3B, the horizontal portion is lower than the bottom surface of the package 4)**; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 3A and 3B, element 12; column 4, lines 37-40)**,

each of said leads having an uppermost end which is lower than an uppermost end of said opening **(Figs. 3A and 3B, Figs. 6A and 6B; top end of leads 6 is lower than top of hole in package 4)**, said level difference having a surface which intersects the side surface of said package, and the surface of said level difference being higher than a bottom surface of said mount **(Fig. 1C, upper surface of level difference 12 is higher than bottom of mount 3)**.

Independent claim 28 recites a semiconductor element module, comprising:

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)**;

a semiconductor element within said package **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 3A and 3B, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Fig. 3B, vertical portion of the leads 6)** and another open end portion having a tip which is downwardly protruded from a plane including a bottom surface of said package and which is oriented in an outward direction relative to said side surface of said package **(Fig. 3B, horizontal portion of the leads 6)**; and

a level difference at said side surface of the package adjacent to said bottom surface of the package so as to form a space between said leads and said package **(Figs. 3A and 3B, element 12; column 4, lines 37-40)**.

Independent claim 33 recites a semiconductor element module, comprising:

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)**;

a semiconductor element within said package **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 2A and 3A, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Figs. 2A and 3A, upper wider portion of the leads 6)** and another open end portion being downwardly protruded from a plane including a bottom surface of said package **(Figs. 2A and 3A, lower narrow portion of the leads 6)**;

a level difference formed by a surface which intersects the side surface of said package adjacent to the bottom surface of said package and which is substantially perpendicular to said side surface and a portion of the leads which protrude downwardly therefrom so as to form a space between said leads and said package **(Figs. 2B and 3B, element 12; column 4, lines 37-40)**; and

a brazing material disposed between the surface of said level difference and the downwardly protruding portion of the leads to secure the attachment of said leads to said package **(Fig. 1C, element 7; column 1, lines 26-28; column 4, lines 1-3)**.

Independent claim 35 recites a semiconductor element module, comprising:

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)** having an opening for allowing an optical signal to pass therethrough **(Fig. 1, opening in package 4 through which optical fiber 2 passes)**;

an optical element located in said package for outputting or inputting the optical signal **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 2A and 3A, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Figs. 2A and 3A, upper wider portion of the leads 6)** and another open

end portion being downwardly protruded from a plane including a bottom surface of said package **(Figs. 2A and 3A, lower narrow portion of the leads 6)**; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 2B and 3B, element 12; column 4, lines 37-40)**;

each of said leads having an uppermost end which is lower than an uppermost end of said opening **(Figs. 2B and 3B, Fig. 6B; top end of leads 6 is lower than top of hole in package 4)**.

Independent claim 36 recites a semiconductor element module, comprising:

a semiconductor element **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a package having walls that surround said semiconductor element **(Figure 1A *et seq.*, element 4; column 4, line 13)**;

a plurality of leads **(Figs. 2A and 3A, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along the exterior surface of a side wall of said package **(Figs. 2A and 3A, upper wider portion of the leads 6)** and another open end portion being downwardly protruded from a plane including a bottom surface of said package **(Figs. 2A and 3A, lower narrow portion of the leads 6)**;

a level difference that forms a recess away from the exterior surface of the side wall of said package adjacent to the bottom surface of said package, said recess having a width which is greater than the thickness of said side wall **(Figs. 2B and 3B, element 12; column 4, lines 37-40)**; and

a brazing material disposed within said recess to secure the attachment of said leads to said package **(Fig. 1C, element 7; column 1, lines 26-28; column 4, lines 1-3)**.

Independent claim 38 recites a semiconductor element module, comprising;

a package having an inner bottom surface **(Figure 1A *et seq.*, element 4; column 4, line 13)** and an opening for allowing an optical signal to pass

therethrough **(Fig. 1, opening in package 4 through which optical fiber 2 passes)**;

an optical element located in said package and supported by said inner bottom surface, for outputting or inputting the optical signal **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 2A and 3A, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Figs. 2A and 3A, upper wider portion of the leads 6)** and another open portion being downwardly protruded from a plane including a bottom surface of said package **(Figs. 2A and 3A, lower narrow portion of the leads 6)**; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 2B and 3B, element 12; column 4, lines 37-40)**,

and wherein each of said leads has an uppermost end which is lower than an uppermost end of said opening **(Figs. 2B and 3B, Figs. 6A and 6B; top end of leads 6 is lower than top of hole in package 4)**, said level difference having a surface which intersects the side surface of said package, and the surface of said level difference being higher than the inner bottom surface of said package **(Fig. 1C, upper surface of level difference 12 is higher than inner bottom surface of package 4)**.

Independent claim 40 recites a semiconductor element module, comprising;

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)** having an opening for allowing an optical signal to pass therethrough **(Fig. 1, opening in package 4 through which optical fiber 2 passes)**;

an optical element located in said package for outputting or inputting the optical signal **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a mount having said optical element placed thereon for fixing said optical element to said package **(Fig. 1B, element 3; column 1, lines 20-21; column 4, lines 1-3)**;

a plurality of leads **(Figs. 3A and 3B, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Figs. 2A and 3A, upper wider portion of the leads 6)** and another open end portion being downwardly protruded from a plane including a bottom surface of said package **(Figs. 2A and 3A, lower narrow portion of the leads 6)**; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 2B and 3B, element 12; column 4, lines 37-40)**,

and wherein each of said leads has an uppermost end which is lower than an uppermost end of said opening **(Figs. 2B and 3B, Figs. 6A and 6B; top end of leads 6 is lower than top of hole in package 4)**, said level difference having a surface which intersects the side surface of said package, and the surface of said level difference being higher than a bottom surface of said mount **(Fig. 1C, upper surface of level difference 12 is higher than bottom of mount 3)**.

Independent claim 42 recites a semiconductor element module, comprising:

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)**;

a semiconductor element within said package **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 2A and 3A, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Figs. 2A and 3A, upper wider portion of the leads 6)** and another open end portion for attachment to a mounting surface, said open end portion being downwardly protruded from a plane including a bottom surface of said package and being shaped to provide a space between the bottom surface of said package and the mounting surface **(Figs. 2A and 3A, lower narrow portion of the leads 6)**;

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 3A and 3B, element 12; column 4, lines 37-40)**; and

a brazing material disposed within said level difference to secure the connection of said leads to said package, to thereby enable said space between the bottom surface of said package and the mounting surface to be no greater than a prescribed amount **(Fig. 1C, element 7; column 1, lines 26-28; column 4, lines 1-3)**.

Independent claim 45 recites a semiconductor device comprising a substrate **(Figs. 3A and 3B, element 8; column 1, lines 33-35; column 4, line 35)** and a semiconductor element module mounted on said substrate, said semiconductor element module including;

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)**;

a semiconductor element within said package **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 2A and 3a, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Figs. 2A and 3A, upper wider portion of the leads 6)** and another open end portion for attachment to a mounting surface, said open end portion being downwardly protruded from a plane including a bottom surface of said package and being shaped to provide a space between the bottom surface of said package and the mounting surface **(Figs. 2A and 3A, lower narrow portion of the leads 6)**;

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 2B and 3B, element 12; column 4, lines 37-40)**; and

a brazing material disposed within said level difference to secure the connection of said leads to said package, to thereby enable said space between the bottom surface of said package and the mounting surface to be no greater than a prescribed amount **(Fig. 1C, element 7; column 1, lines 26-28; column 4, lines 1-3)**.

Independent claim 51 recites a semiconductor device comprising a substrate **(Figs. 3A and 3B, element 8; column 1, lines 33-35; column 4, line 35)** and a semiconductor element module mounted on said substrate,

said substrate having a plurality of through-holes and conductor patterns **(Fig. 2B, element 10; column 1, lines 35-40)**;

said semiconductor element module, including:

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)**;

a semiconductor element within said package **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 2A and 3A, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached to a side surface of said package **(Figs. 2A and 3A, upper wider portion of the leads 6)** and another open end portion being downwardly protruded from a plane including a bottom surface of said package **(Figs. 2A and 3A, lower narrow portion of the leads 6)**, at least one of said plurality of leads being connected to a high frequency terminal of said semiconductor element module **(column 5, lines 47-54)**; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 2B and 3B, element 12; column 4, lines 37-40)**;

wherein each lead connected to a high frequency terminal is surface-mounted onto said conductor pattern, while each of the remaining leads is inserted into said each of said through-holes **(column 5, lines 38-54)**.

Independent claim 52 recites a semiconductor element module, comprising:

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)**;

a semiconductor element within said package **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 4A and 6A, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion of a first width attached along a side surface of said package **(Figs. 4A, 5A and 6A, upper wider portion of leads**

**6; column 4, lines 55-59, and line 65 to column 5, line 2; column 5, lines 22-24)**, an open end portion of a second, narrower width being downwardly protruded from a plane including a bottom surface of said package **(Figs. 4A, 5A and 6A, lower thinner portion of leads 6)**, and a level difference which defines a transition from said first width to said second width **(Figs. 4A, 5A and 6A, level difference 13; column 4, lines 55-59)**; and

a brazing material located at an edge of said package to secure the attachment of said leads to said package **(Fig. 1C, element 7; column 1, lines 26-28; column 4, lines 1-3)**;

wherein said level difference is located lower than said brazing material **(column 5, lines 5-10; Figs. 4C, 5B and 6B)**.

Independent claim 54 recites a semiconductor device, comprising;

a substrate having a mounting surface on which conductor patterns are formed **(Figs. 3A and 3B, element 8; column 1, lines 33-35; column 4, line 35)**; and

a semiconductor element module having:

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)**;

a semiconductor element within said package **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 4A and 6A, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion of a first width attached along a side surface of said package **(Figs. 4A, 5A and 6A, upper wider portion of leads 6; column 4, lines 55-59, and line 65 to column 5, line 2; column 5, lines 22-24)**, an open end portion of a second, narrower width being downwardly protruded from a plane including a bottom surface of said package **(Figs. 4A, 5A and 6A, lower thinner portion of leads 6)**, and a level difference which defines a transition from said first width to said second width **(Figs. 4A, 5A and 6A, level difference 13; column 4, lines 55-59)**, wherein each of said leads is bent at a point below said level difference **(Figs. 6A and 6B; column 5, lines 29-32)**; and

a brazing material located at an edge of said package to secure the attachment of said leads to said package **(Fig. 1C, element 7; column 1, lines 26-28; column 4, lines 1-3)**, wherein said level difference is located lower than said brazing material **(column 5, lines 5-10; Figs. 4C, 5B and 6B)**;

wherein said open end portions of said leads on said semiconductor element module are soldered onto said conductor patterns so that a bottom of said package forms a prescribed space with said mounting surface **(column 5, lines 32-36)**.

Independent claim 56 recites a semiconductor element module, comprising:

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)**;

a semiconductor element within said package **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 4A and 6A, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said semiconductor element to an external circuit, said plurality of leads each having a wide portion connected to a side surface of said package **(Figs. 4A, 5A and 6A, upper wider portion of leads 6; column 4, lines 55-59, and line 65 to column 5, line 2; column 5, lines 22-24)** and a narrow portion that extends downwardly beyond the bottom surface of said package **(Figs. 4A, 5A and 6A, lower thinner portion of leads 6)**, wherein said wide portion extends below the bottom edge of said side surface **(column 4, lines 56-57)**, and

a level difference in said side surface of said package adjacent said bottom surface that forms a space between the wide portion of each lead that extends below the bottom edge of said side surface and the bottom of said package **(Figs. 4A, 5A and 6A, level difference 13; column 4, lines 55-59)**.

Independent claim 59 recites a semiconductor element module, comprising:

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)**;

a semiconductor element within said package **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 3A and 3B, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of

said package **(Fig. 3B, vertical portion of the leads 6)** and another open end portion having a tip which is downwardly protruded from a plane including a bottom surface of said package and which is oriented in an outward direction relative to said side surface of said package **(Fig. 3B, horizontal portion of the leads 6)**;

a level difference at said side surface of said package adjacent to said bottom surface of said package so as to form a space between said leads and said package **(Figs. 3A and 3B, element 12; column 4, lines 37-40)**;

wherein said level difference has a first surface which intersects the side surface of said package and which is substantially perpendicular to said side surface and a portion of the leads which protrude downwardly therefrom, and a second surface which intersects said first surface and which is substantially parallel to said side surface **(Figs. 1A et seq., horizontal and vertical surfaces that define level difference 12)**;

wherein said semiconductor element module further includes a brazing material that is disposed between said first surface and each of the downwardly protruding portions of the leads to secure the attachment of said leads to said package **(Fig. 1C, element 7; column 1, lines 26-28; column 4, lines 1-3)**; and

wherein said brazing material forms a brazed joint fillet that is displaced from said second surface **(Figs. 1C, 2B, 3B, etc., brazing 7 displaced from vertical surface of level difference 12)**.

Independent claim 60 recites a semiconductor device comprising a substrate **(Figs. 3A and 3B, element 8; column 1, lines 33-35; column 4, line 35)** and a semiconductor element module mounted on said substrate, said semiconductor element module including:

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)**;

a semiconductor element within said package **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a plurality of leads **(Figs. 3A and 3B, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package **(Fig. 3B, vertical portion of the leads 6)** and another open end

portion having a tip which is downwardly protruded from a plane including a bottom surface of said package and which is oriented in an outward direction relative to said side surface of said package **(Fig. 3B, horizontal portion of the leads 6)**;

a level difference at said side surface of said package adjacent to said bottom surface of said package so as to form a space between said leads and said package **(Figs. 3A and 3B, element 12; column 4, lines 37-40)**;

wherein said level difference has a first surface which intersects the side surface of said package and which is substantially perpendicular to said side surface and a portion of the leads which protrude downwardly therefrom, and a second surface which intersects said first surface and which is substantially parallel to said side surface **(Figs. 1A et seq., horizontal and vertical surfaces that define level difference 12)**;

wherein said semiconductor element module further includes a brazing material that is disposed between said first surface and each of the downwardly protruding portions of the leads to secure the attachment of said leads to said package **(Fig. 1C, element 7; column 1, lines 26-28; column 4, lines 1-3)**; and

wherein said brazing material forms a brazed joint fillet that is displaced from said second surface **(Figs. 1C, 2B, 3B, etc., brazing 7 displaced from vertical surface of level difference 12)**.

Independent claim 61 recites a semiconductor element module, comprising;

a package **(Figure 1A *et seq.*, element 4; column 4, line 13)** having an opening for allowing an optical signal to pass therethrough **(Fig. 1, opening in package 4 through which optical fiber 2 passes)**;

an optical element located in said package for outputting or inputting the optical signal **(Fig. 1B, optical element 1; column 1, lines 11-12 and 17-19; column 4, lines 10-13)**;

a mount disposed between said optical element and said package **(Fig. 1B, element 3; column 1, lines 20-21; column 4, lines 1-3)**;

a plurality of leads **(Figs. 3A and 3B, leads 6; column 1, lines 23-26; column 4, line 43)** for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said

package **(Fig. 3B, vertical portion of the leads 6)** and another open end portion bent in an outward direction relative to the side surface of said package **(Fig. 3B, horizontal portion of the leads 6)**, said open end portion being downwardly protruded from a plane including a bottom surface of said package **(Fig. 3B, the horizontal portion is lower than the bottom surface of the package 4)**; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package **(Figs. 3A and 3B, element 12; column 4, lines 37-40)**,

each of said leads having an uppermost end which is lower than an uppermost end of said opening **(Figs. 3A and 3B, Figs. 6A and 6B; top end of leads 6 is lower than top of hole in package 4)**, said level difference having a surface which intersects the side surface of said package, and the surface of said level difference being higher than a bottom surface of said mount **(Fig. 1C, upper surface of level difference 12 is higher than bottom of mount 3)**.

## VI. Grounds of Rejection to be Reviewed on Appeal

The final Office Action presents a single ground of rejection for review on this appeal:

Claims 11-47, 51-54 and 56-62 stand finally rejected under 35 U.S.C. 251 on the grounds that they are considered to be "an improper recapture of broadened claimed subject matter surrendered in the application for the patent upon which the present reissue is based." (Final Office Action dated April 7 2008, at page 2)

## VII. Argument

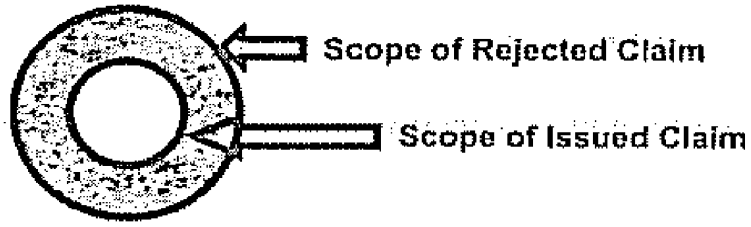
Since the basis for the rejection is common to all appealed claims, a detailed discussion of the rejection will be presented with respect to independent claims 11 and 52, together with a briefer discussion of at least one reason why the rejection is unfounded for each of the other independent claims.

Reissue claims 11-62 were rejected under 35 U.S.C. §251. The Office Action states that each of the patented independent claims (claims 1-10) recites language such as "wherein said level difference serves to avoid capillary flow of solder to

prevent short-circuiting between the leads adjacent to each other". The Action goes on to conclude that, since this recitation does not appear in the independent claims added via reissue, Applicants are attempting to recapture surrendered subject matter. In making this assessment, the Office Action is employing an improper point of reference to determine the subject matter that was surrendered.

In essence, the Office Action is taking the position that it is impermissible for a reissue claim to omit a recitation that was added subsequent to a rejection in the original application, under the rule against recapture. However, this is not the correct standard. The specific issue involved herein was addressed by an expanded panel of the Board of Patent Appeals and Interferences in the case of *Ex parte Eggert*, 67 USPQ2d 1716 (Bd. Pat. App. & Inter. 2003). The Board was requested to adopt the position espoused in the final Office Action being appealed herein, but declined to do so. In reaching its decision, the Board indicated that the subject matter that was *surrendered* by a patentee is measured with reference to the rejected claim that existed *prior* to amendment, rather than the amended claim that issued in the patent.

In explaining their decision, the members of the Board employed the following drawing:




**Drawing 1**

In this drawing, the scope of the rejected claim is the outer circle, and the scope of the amended issued claim is the inner circle. The shaded area between the circles represents subject matter which is narrower than the scope of the rejected claim, but broader than the scope of the issued claim. The Board stated, "the surrendered subject matter is the outer circle of Drawing 1 because it is the subject matter appellants conceded was unpatentable." 67 USPQ2d at 1717. It went on to state

that the Examiner was never directly presented with a claim that fell within the scope of the shaded area, and therefore the patentees could not be deemed to have surrendered a claim of that scope. The Board concluded:

> the focus for determining the reach of the reissue recapture rule should be the claim from which the issued claimed [sic] directly evolved, not the issued claim itself. 67 USPQ2d at 1718.

The Board also discussed earlier cases pertaining to the rule against recapture. Quoting from *Ball Corp. v. United States*, 729 F.2d 1429, 221 USPQ 289 (Fed. Cir. 1984), the Board stated that this case establishes that "[t]he proper focus is on the *scope* of the claims, not on the individual *feature* or *element* purportedly given up during prosecution of the original application." 67 USPQ2d at 1724 (emphasis in original). With reference to *Mentor Corp. v. Coloplast, Inc.*, 998 F.2d 992, 27 USPQ2d 1521 (Fed. Cir. 1993), the Board quoted "[t]he recapture rule bars the patentee from acquiring, through reissue, claims that are of the *same* or of *broader scope* than those claims that were cancelled from the original application". *Id.* (emphasis in original).

This same thought was reiterated in the more recent case of *In re Clement*, 45 USPQ2d 1161 (Fed. Cir. 1997), cited in the final Office Action. The court stated "If the scope of the reissue claim is the same as or broader than that of the *canceled* claim, then the patentee is clearly attempting to recapture surrendered subject matter…" *Id.*, at 1164 (emphasis added).

The final Office Action does not meet its burden of showing that the patentee is attempting to recapture surrendered subject matter under the standard set forth in this line of cases. Specifically, there is no showing that any of claims 11-47, 51-54 and 56-62 is the same as, or broader than, the claims that were effectively canceled during the examination of the original application that resulted in the issued patent. For the reasons presented hereinafter, the appealed claims are narrower in scope than the original claims that were effectively canceled.

A. Claim 11

Reissue claim 11 most closely corresponds to claim 1 of the application that matured into the patent. The following table compares rejected claim 1 of the original application with independent reissue claim 11.

| Rejected claim 1 | Claim 11 from reissue application |
|---|---|
| A semiconductor element module, comprising: | A semiconductor element module, comprising: |
| a package, a semiconductor element arranged on said package; and | a package;<br>a semiconductor element within said package; |
| a plurality of leads provided on sides of the package so that an opening end of each said leads is oriented to the side of a package attaching plane, and serving to connect said semiconductor element to an external circuit; | a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion bent in an outward direction relative to the side surface of said package, said open end portion being downwardly protruded from a plane including a bottom surface of said package; and |
| wherein a level differences is provided on the side of said package attaching plane of each of package sides so that a space is formed from each said plurality of leads; and | a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package. |
| wherein said level difference serves to prevent the short-circuiting between the leads adjacent to each other. | |

From this illustration, it can be seen that reissue claim 11 recites each of the structural components present in original claim 1, namely a package, a semiconductor element, a plurality of leads on a side surface of the package to connect the semiconductor element to an external circuit, and a level difference on the side surface of the package to form a space between the leads and the package. In addition, reissue claim 11 further recites that the leads have an open end portion

that is "bent in an outward direction relative to the side surface of said package", and that this open end portion is "downwardly protruded from a plane including a bottom surface of said package", which were not recited in original claim 1. Claim 11 is therefore narrower than the scope of original claim 1 in these respects, i.e. it falls within the shaded area of the figure from the *Eggert* case. Consequently, Applicants are not attempting to recapture the same subject matter that was surrendered during the examination of the original patent application. In other words, they are not attempting to obtain a claim of the same scope as original claim 1 that was rejected and effectively cancelled.

The one recitation that appears in original claim 1 that is not present in reissue claim 11 is "wherein said level difference serves to prevent the short-circuiting between the leads adjacent to each other." This recitation does not define a structural feature that limits the scope of the claim. Rather, it states a result that flows from the presence of the claimed level difference that forms a space between the leads and the package. It does not specify how that result is achieved, and therefore does not operate to limit the claimed structure. As such, the absence of the recitation does not alter the scope of the claim.

Consequently, reissue claim 11 is not the same as, or broader than, rejected claim 1 as it existed prior to amendment. The final Office Action has not presented any evidence that suggests otherwise. It only refers to recitations that were present in the claims *after* they were amended, and subsequently allowed. These additional recitations have no bearing on the subject matter that was *surrendered* by Appellants during the examination of the original patent.

B. Claims 16, 21, 22, 24, 25, 27, 28, 59, 60 and 61

For the same reasons, the other independent claims do not attempt to capture subject matter that was surrendered when the claims of the original application were amended. Specifically, each of reissue claims 16, 21, 22, 24, 25, 27, 28, 59, 60 and 61 recites, among other features, that an open end portion of the lead is bent, or oriented, in an outward direction relative to the side surface of the package, and protrudes downwardly from a plane at the bottom surface of the package. This

feature was not recited in the original claims that were rejected, and represents a narrowing aspect of these reissue claims.

C. Claim 33

Reissue claim 33 recites that the level difference intersects the side surface of the package and is substantially perpendicular to the side surface and a portion of the leads which protrude downwardly therefrom. This feature was not recited in the original claims that were rejected, and represents a narrowing aspect of this reissue claim.

D. Claims 35, 38 and 40

Reissue claims 35, 38 and 40 recite that the package has an opening, and that the leads have an uppermost end which is lower than an uppermost end of the opening. This feature was not recited in the original claims that were rejected, and represents a narrowing aspect of these reissue claims.

E. Claim 36

Reissue claim 36 recites that the level difference forms a recess away from the exterior surface of the sidewall of the package, with this recess having a width which is greater than the thickness of the sidewall. This feature was not recited in the original claims that were rejected, and represents a narrowing aspect of this reissue claim.

F. Claim 38

Reissue claim 38 recites that the surface of the level difference is higher than the inner bottom surface of the package. This feature was not recited in the original claims that were rejected, and represents a narrowing aspect of this reissue claim.

G. Claim 40

Reissue claim 40 recites that the surface of the level difference is higher than the bottom surface of a mount on which the optical element is placed. This feature was not recited in the original claims that were rejected, and represents a narrowing aspect of this reissue claim.

H. Claims 42 and 45

Reissue claims 42 and 45 recite that the open end portion of the leads is shaped to provide a space between the bottom surface of the package and the surface on which the semiconductor element is mounted. This feature was not recited in the original claims that were rejected, and represents a narrowing aspect of these reissue claims.

I. Claim 51

Reissue claim 51 recites that at least one of the plurality of leads is connected to a high frequency terminal of the semiconductor element module, and that this lead is surface-mounted onto a conductor pattern on the substrate. This feature was not recited in the original claims that were rejected, and represents a narrowing aspect of this reissue claim.

J. Claim 56

Claim 56 recites that each of the leads has a wide portion that extends below the bottom edge of the side surface of the package. This feature was not recited in the original claims that were rejected, and represents a narrowing aspect of this reissue claim.

This identification of features in each of subsections B-J above is not intended to be exhaustive of all of the differences between the new reissue claims and the claims of the original application. Rather, these features are illustrative of at least one example in which each independent claim is narrower in scope than the original rejected claims.

K. Claim 52

Claims 52 and 54 differ from the remaining independent claims in that they do not recite a level difference at the side surface of the package. Rather, they recite that the leads have a level difference which defines a transition from a first width to a second width. Claim 52 corresponds most closely to claim 5 of the original patent application. The following table compares rejected claim 5 of the original application with pending claim 52 of the reissue application.

| Rejected claim 5 | Claim 52 from reissue application |
|---|---|
| A semiconductor element module, comprising:<br>a package; and<br>a semiconductor element arranged on said package;<br>a plurality of leads provided on sides of the package so that an opening terminal of each said leads is oriented to a side of a package attaching plane and serving to connect said semiconductor element to an external circuit;<br>wherein a level difference is provided at a portion of each said leads not connected to said package so that the width of each said leads on the side where the lead and package are connected is thick and that on a side of its open end is thin; and<br>wherein said level difference serves to avoid to prevent short-circuiting between the leads adjacent to each other. | A semiconductor element module, comprising:<br>a package;<br>a semiconductor element within said package;<br>a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion of a first width attached along a side surface of said package, an open end portion of a second, narrower width being downwardly protruded from a plane including a bottom surface of said package, and a level difference which defines a transition from said first width to said second width; and<br>a brazing material located at an edge of said package to secure the attachment of said leads to said package;<br>wherein said level difference is located lower than said brazing material. |

From this table, it can be seen that reissue claim 52 recites each of the structural components that are present in original claim 5, namely a package, a semiconductor element, and a plurality of leads having a level difference that distinguishes a thick (wide) portion connected to the package and a thin (narrow) portion at an open end. Moreover, claim 52 recites a brazing material and the location of the level difference relative to the brazing material, which are not recited in original claim 5.

The one explicit recitation of claim 5 that is missing from claim 52 is that the level difference serves to prevent the short-circuiting between adjacent leads.

Similar to the discussion in preceding subsection A, this recitation does not define a structural feature that limits the scope of the claim. Rather, it states a result that flows from the presence of the claimed level difference in the leads. It does not specify how that result is achieved, and therefore does not operate to limit the claimed structure. As such, the absence of the recitation does not improperly broaden the scope of reissue claim 52 beyond that of original claim 5.

Consequently, reissue claim 52 is not the same as, or broader than, rejected claim 5 as it existed prior to amendment. The final Office Action has not presented any evidence that suggests otherwise, since it only refers to recitations that were present in the claims *after* they were amended.

L. Claim 54

Reissue claim 54 recites that each of the leads has a level difference, and is bent at a point below the level difference. This feature was not recited in the original claims that were rejected, and represents a narrowing aspect of this reissue claim.

M. Conclusion

From the foregoing, it can be seen that each of the claims presented for reissue is not of the same, or broader, scope than the claims of the original application that were rejected and thereafter amended. Consistent with the holdings of the *Eggert* case and its predecessor cases that dealt with this issue, Applicants are not attempting to recapture the same subject matter that was surrendered during the examination of the original application. The reissue claims fall within the shaded area of the figure that the Board used to illustrate the proper point of reference when evaluating the rule against recapture. The final Office Action has not provided any evidence to show that any of the reissue claims on appeal are the same as, or broader than, the claims that were *rejected* during examination and effectively canceled by amendment thereof. At best, it only demonstrates that the reissue claims may be broader than the claims that *issued* in the patent. As such, it fails to meet the standard for a proper showing under the rule against recapture.

The rejection under 35 U.S.C. §251 is not properly founded in the statute, and should be reversed.

VIII. Claims Appendix

See attached Claims Appendix for a copy of the claims involved in the appeal.

IX. Evidence Appendix

(none)

X. Related Proceedings Appendix

(none)

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

Date December 10, 2008

By: /James A. LaBarre/
James A. LaBarre
Registration No. 28632

P.O. Box 1404
Alexandria, VA 22313-1404
703 836 6620

## VIII. CLAIMS APPENDIX

**The Appealed Claims**

11. A semiconductor element module, comprising:

a package;

a semiconductor element within said package;

a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion bent in an outward direction relative to the side surface of said package, said open end portion being downwardly protruded from a plane including a bottom surface of said package; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package.

12. A semiconductor element module according to claim 11, further comprising a brazing material disposed within said level difference to secure the attachment of said leads to said package.

13. A semiconductor element module according to claim 12, wherein said brazing material is disposed at a location remote from the bottom surface of said package.

14. A semiconductor element module according to claim 11 wherein said leads extend along and are attached to a side surface of said package.

15. A semiconductor element module according to claim 11, wherein said semiconductor element is an optical element.

16. A semiconductor device comprising a substrate and a semiconductor element module mounted on said substrate, said semiconductor element module including:

a package;

a semiconductor element within said package;

a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion bent in an outward direction relative to the side surface of said package, said open end portion being downwardly protruded from a plane including a bottom surface of said package; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package.

17. A semiconductor device according to claim 16, wherein said substrate has a mounting surface and conductor patterns formed on said mounting surface, said semiconductor element module being mounted on said substrate by joining said open end portions of said leads to said conductor patterns.

18. A semiconductor device according to claim 16, further comprising a brazing material disposed within said level difference to secure the connection of said leads to said package.

19. A semiconductor device according to claim 16, wherein said semiconductor element is an optical element.

20. A semiconductor device according to claim 16, wherein said substrate has a mounting surface, said semiconductor element module being mounted on said substrate so that the bottom surface of said package is spaced from said mounting surface of said substrate by a prescribed distance.

21. A semiconductor element module, comprising:

a package having an opening for allowing an optical signal to pass therethrough;

an optical element located in said package for outputting or inputting the optical signal;

a plurality of leads for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion bent in an outward direction relative to the side surface of said package, said open end portion being downwardly protruded from a plane including a bottom surface of said package; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package,

each of said leads having an uppermost end which is lower than an uppermost end of said opening.

22. A semiconductor element module, comprising;

a package having an inner bottom surface and an opening for allowing an optical signal to pass therethrough;

an optical element located in said package for outputting or inputting the optical signal;

a plurality of leads for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion bent in an outward direction relative to the side surface of said package, said open end portion being downwardly protruded from a plane including a bottom surface of said package; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package,

each of said leads having an uppermost end which is lower than an uppermost end of said opening, said level difference having a surface which intersects the side surface of said package, and the surface of said level difference being higher than the inner bottom surface of said package.

23. A semiconductor element module according to claim 22, further comprising a brazing material disposed within said level difference to secure the attachment of said leads to said package.

24. A semiconductor device comprising a substrate and a semiconductor element module mounted on said substrate,

said semiconductor element module including;

a package having an inner bottom surface and an opening for allowing an optical signal to pass therethrough;

an optical element located in said package for outputting or inputting the optical signal;

a plurality of leads for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion bent in an outward direction relative to the side surface of said package, said open end portion being downwardly protruded from a plane including a bottom surface of said package; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package,

each of said leads having an uppermost end which is lower than an uppermost end of said opening, said level difference having a surface which intersects the side surface of said package, and the surface of said level difference being higher than the inner bottom surface of said package.

25. A semiconductor element module, comprising;

a package having an opening for allowing an optical signal to pass therethrough;

an optical element located in said package for outputting or inputting the optical signal;

a mount having said optical element placed thereon for fixing said optical element to said package;

a plurality of leads for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion bent in an outward direction relative to the side surface of said package, said open end portion being downwardly protruded from a plane including a bottom surface of said package; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package,

each of said leads having an uppermost end which is lower than an uppermost end of said opening, said level difference having a surface which

intersects the side surface of said package, and the surface of said level difference being higher than a bottom surface of said mount.

26. A semiconductor element module according to claim 25, further comprising a brazing material disposed within said level difference to secure the attachment of said leads to said package.

27. A semiconductor device comprising a substrate and a semiconductor element module mounted on said substrate,

said semiconductor element module including;

a package having an opening for allowing an optical signal to pass therethrough;

an optical element located in said package for outputting or inputting the optical signal;

a mount having said optical element placed thereon for fixing said optical element to said package;

a plurality of leads for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion bent in an outward direction relative to the side surface of said package, said open end portion being downwardly protruded from a plane including a bottom surface of said package; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package,

each of said leads having an uppermost end which is lower than an uppermost end of said opening, said level difference having a surface which intersects the side surface of said package, and the surface of said level difference being higher than a bottom surface of said mount.

28. A semiconductor element module, comprising:

a package;

a semiconductor element within said package;

a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion having a tip which is downwardly protruded from a plane including a bottom surface of said package and which is oriented in an outward direction relative to said side surface of said package; and

a level difference at said side surface of the package adjacent to said bottom surface of the package so as to form a space between said leads and said package.

29. A semiconductor element module according to claim 28, further comprising a brazing material disposed within said level difference to secure the attachment of said leads to said package.

30. A semiconductor element module according to claim 28, wherein said level difference has a surface which intersects the side surface of said package and which is substantially perpendicular to said side surface and a portion of the leads which protrude downwardly therefrom, and further including a brazing material which is disposed between the surface of said level difference and the downwardly protruding portion of the leads to secure the attachment of said leads to said package.

31. A semiconductor element module according to claim 28, wherein each of said leads has an uppermost end, and a distance between the bottom surface of said package and the uppermost end of each of said leads is larger than the distance between the tip of the open end of each of said leads and the bottom surface of said package.

32. A semiconductor element module according to claim 28, wherein said level difference has a surface which intersects the side surface of said package, and a distance between the bottom surface of said package and the surface of said level difference is larger than the distance between the tip of the open end of each of said leads and the bottom surface of said package.

33. A semiconductor element module, comprising:

a package;

a semiconductor element within said package;

a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion being downwardly protruded from a plane including a bottom surface of said package;

a level difference formed by a surface which intersects the side surface of said package adjacent to the bottom surface of said package and which is substantially perpendicular to said side surface and a portion of the leads which protrude downwardly therefrom so as to form a space between said leads and said package; and

a brazing material disposed between the surface of said level difference and the downwardly protruding portion of the leads to secure the attachment of said leads to said package.

34. A semiconductor element module according to claim 33, wherein said brazing material is disposed at a location remote from the bottom surface of said package.

35. A semiconductor element module, comprising:

a package having an opening for allowing an optical signal to pass therethrough;

an optical element located in said package for outputting or inputting the optical signal;

a plurality of leads for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion being downwardly protruded from a plane including a bottom surface of said package; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package,

each of said leads having an uppermost end which is lower than an uppermost end of said opening.

36. A semiconductor element module, comprising: a semiconductor element; a package having walls that surround said semiconductor element;

a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along the exterior surface of a side wall of said package and another open end portion being downwardly protruded from a plane including a bottom surface of said package;

a level difference that forms a recess away from the exterior surface of the side wall of said package adjacent to the bottom surface of said package, said recess having a width which is greater than the thickness of said side wall; and

a brazing material disposed within said recess to secure the attachment of said leads to said package.

37. A semiconductor element module according to claim 36, wherein said brazing material is disposed at a location remote from the bottom surface of said package.

38. A semiconductor element module, comprising;

a package having an inner bottom surface and an opening for allowing an optical signal to pass therethrough;

an optical element located in said package and supported by said inner bottom surface, for outputting or inputting the optical signal;

a plurality of leads for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open portion being downwardly protruded from a plane including a bottom surface of said package; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package,

and wherein each of said leads has an uppermost end which is lower than an uppermost end of said opening, said level difference having a surface which intersects the side surface of said package, and the surface of said level difference being higher than the inner bottom surface of said package.

39. A semiconductor element module according to claim 38, further comprising a brazing material disposed within said level difference to secure the attachment of said leads to said package.

40. A semiconductor element module, comprising;

a package having an opening for allowing an optical signal to pass therethrough;

an optical element located in said package for outputting or inputting the optical signal;

a mount having said optical element placed thereon for fixing said optical element to said package;

a plurality of leads for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion being downwardly protruded from a plane including a bottom surface of said package; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package,

and wherein each of said leads has an uppermost end which is lower than an uppermost end of said opening, said level difference having a surface which intersects the side surface of said package, and the surface of said level difference being higher than a bottom surface of said mount.

41. A semiconductor element module according to claim 40, further comprising a brazing material disposed within said level difference to secure the attachment of said leads to said package.

42. A semiconductor element module, comprising:

a package;

a semiconductor element within said package;

a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion for attachment to a mounting surface, said open end portion being downwardly protruded from a plane including a bottom surface of said package and being shaped to provide a space between the bottom surface of said package and the mounting surface;

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package; and

a brazing material disposed within said level difference to secure the connection of said leads to said package, to thereby enable said space between the bottom surface of said package and the mounting surface to be no greater than a prescribed amount.

43. A semiconductor element module according to claim 42, wherein said shape comprises an outward bending of the open end portion of the leads to define a mounting plane that is substantially parallel to said bottom surface at said prescribed distance therefrom.

44. A semiconductor element module according to claim 42, wherein said shape comprises a transition in the width of said leads that defines an abutment at said prescribed distance below the bottom surface of said package.

45. A semiconductor device comprising a substrate and a semiconductor element module mounted on said substrate, said semiconductor element module including;

a package;

a semiconductor element within said package;

a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion for attachment to a mounting surface, said open end portion being downwardly protruded from a plane including a bottom surface of said package and being shaped to provide a space between the bottom surface of said package and the mounting surface;

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package; and

a brazing material disposed within said level difference to secure the connection of said leads to said package, to thereby enable said space between the

bottom surface of said package and the mounting surface to be no greater than a prescribed amount.

46. A semiconductor element module according to claim 45, wherein said shape comprises an outward bending of the open end portion of the leads to define a mounting plane that is substantially parallel to said bottom surface at said prescribed distance therefrom.

47. A semiconductor element module according to claim 45, wherein said shape comprises a transition in the width of said leads that defines an abutment at said prescribed distance below the bottom surface of said package.

51. A semiconductor device comprising a substrate and a semiconductor element module mounted on said substrate,

said substrate having a plurality of through-holes and conductor patterns;

said semiconductor element module, including:

a package;

a semiconductor element within said package;

a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached to a side surface of said package and another open end portion being downwardly protruded from a plane including a bottom surface of said package, at least one of said plurality of leads being connected to a high frequency terminal of said semiconductor element module; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package;

wherein each lead connected to a high frequency terminal is surface-mounted onto said conductor pattern, while each of the remaining leads is inserted into said each of said through-holes.

52. A semiconductor element module, comprising:

a package;

a semiconductor element within said package;

a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion of a first width attached along a side surface of said package, an open end portion of a second, narrower width being downwardly protruded from a plane including a bottom surface of said package, and a level difference which defines a transition from said first width to said second width; and

a brazing material located at an edge of said package to secure the attachment of said leads to said package;

wherein said level difference is located lower than said brazing material.

53. A semiconductor element module according to claim 52, wherein each of said leads is bent at a point below said level difference.

54. A semiconductor device, comprising;

a substrate having a mounting surface on which conductor patterns are formed; and

a semiconductor element module having:

a package;

a semiconductor element within said package;

a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion of a first width attached along a side surface of said package, an open end portion of a second, narrower width being downwardly protruded from a plane including a bottom surface of said package, and a level difference which defines a transition from said first width to said second width, wherein each of said leads is bent at a point below said level difference; and

a brazing material located at an edge of said package to secure the attachment of said leads to said package, wherein said level difference is located lower than said brazing material;

wherein said open end portions of said leads on said semiconductor element module are soldered onto said conductor patterns so that a bottom of said package forms a prescribed space with said mounting surface.

56. A semiconductor element module, comprising:

a package;

a semiconductor element within said package;

a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having a wide portion connected to a side surface of said package and a narrow portion that extends downwardly beyond the bottom surface of said package, wherein said wide portion extends below the bottom edge of said side surface, and

a level difference in said side surface of said package adjacent said bottom surface that forms a space between the wide portion of each lead that extends below the bottom edge of said side surface and the bottom of said package.

57. The semiconductor package of claim 56, further including a brazing material disposed within said level difference for securing the connection of said leads to said package.

58. The semiconductor package of claim 56, wherein said narrow portions of said leads are bent outwardly away from said package to form a mounting surface.

59. A semiconductor element module, comprising:

a package;

a semiconductor element within said package;

a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion having a tip which is downwardly protruded from a plane including a bottom surface of said package and which is oriented in an outward direction relative to said side surface of said package;

a level difference at said side surface of said package adjacent to said bottom surface of said package so as to form a space between said leads and said package;

wherein said level difference has a first surface which intersects the side surface of said package and which is substantially perpendicular to said side surface and a portion of the leads which protrude downwardly therefrom, and a second surface which intersects said first surface and which is substantially parallel to said side surface;

wherein said semiconductor element module further includes a brazing material that is disposed between said first surface and each of the downwardly protruding portions of the leads to secure the attachment of said leads to said package; and

wherein said brazing material forms a brazed joint fillet that is displaced from said second surface.

60. A semiconductor device comprising a substrate and a semiconductor element module mounted on said substrate, said semiconductor element module including:

a package;

a semiconductor element within said package;

a plurality of leads for connecting said semiconductor element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion having a tip which is downwardly protruded from a plane including a bottom surface of said package and which is oriented in an outward direction relative to said side surface of said package;

a level difference at said side surface of said package adjacent to said bottom surface of said package so as to form a space between said leads and said package;

wherein said level difference has a first surface which intersects the side surface of said package and which is substantially perpendicular to said side surface and a portion of the leads which protrude downwardly therefrom, and a second

surface which intersects said first surface and which is substantially parallel to said side surface;

wherein said semiconductor element module further includes a brazing material that is disposed between said first surface and each of the downwardly protruding portions of the leads to secure the attachment of said leads to said package; and

wherein said brazing material forms a brazed joint fillet that is displaced from said second surface.

61. A semiconductor element module, comprising;

a package having an opening for allowing an optical signal to pass therethrough;

an optical element located in said package for outputting or inputting the optical signal;

a mount disposed between said optical element and said package;

a plurality of leads for connecting said optical element to an external circuit, said plurality of leads each having one end portion attached along a side surface of said package and another open end portion bent in an outward direction relative to the side surface of said package, said open end portion being downwardly protruded from a plane including a bottom surface of said package; and

a level difference at the side surface of said package adjacent to the bottom surface of said package so as to form a space between said leads and said package,

each of said leads having an uppermost end which is lower than an uppermost end of said opening, said level difference having a surface which intersects the side surface of said package, and the surface of said level difference being higher than a bottom surface of said mount.

62. A semiconductor element module according to claim 61, further comprising a brazing material disposed within said level difference to secure the attachment of said leads to said package.